Japanese Patent Application Laid-Open No. 6-324866

[TITLE OF THE INVENTION]

BRANCH DIRECTION PREDICTING DYNAMIC CHANGING APPARATUS

[ABSTRACT]

[OBJECT]

When performing the branch direction prediction of the branch command having no executing record, the present invention prevents reduction of the processing speed caused by lowering of the success rate of the branch direction prediction of the branch command by using a method of a branch command of a program.

[CONSTITUTION]

The determination of the branch direction predicted value is carried out by comparing the value obtained by subtracting the value of the branch direction prediction failure counter 4 from the value of the branch command counter 3 with the value of the branch direction prediction failure counter 4 with as a start of the input signal of the branch direction prediction measuring timer 6. If it is found that the value obtained by subtracting the value of the branch direction prediction failure counter 4 from the value of the branch command counter 3 is smaller than the value of the branch direction prediction failure counter 4 from the result of the comparison, the branch direction predicted value determination circuit 7 outputs the branch direction predicted value controlling signal to the branch direction predicted value register 8.

[CLAIMS]

[Claim 1]

A branch direction predicting dynamic changing apparatus comprising:

branch direction predicted value storing means for storing a predicted value of a branch direction of a branch command;

branch direction predicting means for comparing the branch direction, which is indicated by the predicted value from said branch direction predicted value storing means with the branch direction of the branch command to be processed;

number counting means for counting at least one of the number of a prediction failure and the number of a prediction success on the basis of the signal from said branch direction predicting means; and

branch direction predicted value determining means for determining whether the number of the prediction failure is more than the number of a prediction success or not during period of counting time on the basis of the counted value from said number counting means and outputting the signal indicating that the number of the prediction failure is more than the number of a prediction success to switch the predicted branch direction of the branch direction predicted value, which is stored in said branch direction predicted value storing means.

[Claim 2]

A branch direction predicting dynamic changing apparatus according to claim 1 comprising:

branch command determining means for determining whether

the command comprises a branch command for every executing process or not; and

branch command counting means for counting the number of the branch commands in response to the determining result in said branch determining means;

wherein said number counting means counts the number of the prediction failure;

said branch direction predicted value determining means subtracts the number of the prediction failure, which is counted by said number counting means from the number of the branch commands, which is counted by said branch command counting means to obtain the number of the prediction success and determines whether the obtained number of the prediction success is less than said number of the prediction failure or not.

[Claim 3]

A branch direction predicting dynamic changing apparatus according to claim 1 wherein said number counting means counts both of the number of the prediction failure and the number of the prediction success;

said branch direction predicted value determining means determines whether the number of the prediction failure, which is given by said number counting means during period of time is more than said number of the prediction success, which is given by said number counting means or not.

[Claim 4]

A branch direction predicting dynamic changing apparatus according to claim 1 comprising:

branch command determining means for determining whether the command comprises a branch command for every executing process or not; and

branch command counting means for counting the number of the branch commands in response to the determining result in said branch determining means;

wherein said number counting means counts the number of the prediction success;

said branch direction predicted value determining means subtracts the number of the prediction success, which is counted by said number counting means from the number of the branch commands, which is counted by said branch command counting means to obtain the number of the prediction failure and determines whether the obtained number of the prediction failure is more than said number of the prediction success or not.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[TECHNICAL FILED TO WHICH THE INVENTION PERTAINS]

The present invention relates to a branch direction predicting dynamic changing apparatus for changing the branch direction predicting direction of the branch command dynamically on an information processing apparatus for predicting a branch direction of a branch command and performing a branch direction predicting success processing at higher speed than the branch direction predicting failure processing.

[0002]

[PRIOR ART]

A typical example for this kind of the branch direction prediction is disclosed in Japanese Patent Application Laid-Open No. 3-73022. As shown in FIG. 6, a branch predicting circuit is employed by using a high probability that a general program is branched again by the branch command in the same place. Further, by using the features of the program, i.e., " a high probability that the backward branch occurs repeatedly" and " the probability that the forward branch is repeated mainly depends on the program" , the address of the branch command is compared with the address of the branched destination.

[0003]

With respect to the branch command which is executed at the first time and the previous branch direction is unknown, a hardware of the information processing apparatus fixedly have been predicted the branch direction.

[0004]

[PROBLEM TO BE SOLVED BY THE INVENTION]

The branch direction prediction of the branch command is generally performed in order to process the software command execution at a high speed. In the case that the branch direction prediction fails, the processing grows late comparing with the case that the branch direction prediction achieves success.

[0005]

In the above described conventional branch direction prediction of the branch command, when the hardware predicts the branch direction fixedly, even using the program with the

same logic, there is a difference in processing time of the program depending on the branch command using method of the program. Accordingly, when the program is created so as to process at a high speed, there is a defect that it is necessary to consider the branch direction of the branch command that the hardware predicts the branch direction fixedly to use the branch command.

[0006]

[MEANS FOR SOLVING PROBLEM]

In order to solve the above mentioned problems, a first branch direction predicting dynamically changing apparatus according to the present invention includes a branch direction predicted value register for storing a predicted value of a branch direction of a branch command, a branch direction predicting circuit for comparing the branch direction, which is indicated by the predicted value from this branch direction predicted value register with the branch direction of the branch command to be processed, a counter for counting at least one of the number of a prediction failure and the number of a prediction success on the basis of the signal from this branch direction predicting circuit and a branch direction predicted value determining circuit for determining whether the number of the prediction failure is more than the number of a prediction success or not during period of counting time on the basis of the counted value from this counter and outputting the signal indicating that the number of the prediction failure is more than the number of a prediction success to switch the predicted

branch direction of the branch direction predicted value, which is stored in the branch direction predicted value register.

[0007]

In order to solve the above mentioned problem, a second branch direction predicting dynamically changing apparatus according to the present invention includes a branch command determination circuit for determining whether the software command comprises a branch command or not every for execution processing of the software command, a branch command counter for adding in response to a branch command determination signal in this branch command determination circuit, a branch direction predicting circuit for outputting a branch direction prediction failure signal when the branch direction of the branch command is not identical with the branch direction indicated by a predicted value from the branch direction predicted value register on the basis of the determination result from the branch command determination circuit, a branch direction prediction failure counter for counting the branch direction prediction failure signal from this branch direction predicting circuit and obtaining the number of failure of the branch direction prediction, a timer for clocking period of time in reference to a counting time of the branch direction prediction success and the branch direction prediction failure, a branch direction predicted value determination circuit for outputting a signal to switch the predicted branch direction of the branch direction predicted value when the number of the prediction failure from the branch direction prediction

failure counter which is counted during period of time indicated by this timer is compared with the number of prediction success obtained by subtracting the number of the prediction failure from the number of the branch commands from the branch command counter and this number of the prediction failure is more than the number of prediction success, and a branch direction predicted value register for storing the branch direction predicted value indicating the predicted branch direction and switching the branch predicted value to the direction of the failure when the signal is given to indicate that the number of the prediction failure from the foregoing branch direction predicted value determination circuit is more than the number of prediction success.

[0008]

In order to solve the above mentioned problem, a third branch direction predicting dynamically changing apparatus according to the present invention includes a branch command determination circuit for determining whether the software command comprises a branch command or not every for execution processing of the software command, a branch direction predicting circuit for outputting a branch direction prediction failure signal when the branch direction of the branch command is not identical with the branch direction indicated by a predicted value from the branch direction predicted value register on the basis of this determination result from the branch command determination circuit and on the contrary outputting a branch direction prediction success

signal when identical, a branch direction prediction failure counter for counting the branch direction prediction failure signal from this branch direction predicting circuit and obtaining the number of failure of the branch direction prediction, a branch direction prediction failure counter for counting the prediction failure signal from the branch direction predicting circuit and obtaining the number of the failure of the branch direction prediction ,a branch direction prediction success counter for counting the prediction success signal from the foregoing branch direction predicting circuit and obtaining the number of the success of the branch direction prediction, a timer for clocking period of time in reference to a counting time of the branch direction prediction success and the branch direction prediction failure, a branch direction predicted value determination circuit for outputting a signal to switch the predicted branch direction of the branch direction predicted value when the number of the prediction failure from the branch direction prediction failure counter which is counted within a time indicated by this timer is compared with the number of prediction success from the foregoing branch command counter and this number of the prediction failure is more than the number of prediction success, and a branch direction predicted value register 8 for storing the branch direction predicted value indicating the predicted branch direction and switching the predicted branch direction of the branch predicted value by the signal indicating that the number of the prediction failure from the foregoing branch direction

predicted value determination circuit is more than the number of prediction success.

[0009]

In order to solve the above mentioned problem, a fourth branch direction predicting dynamically changing apparatus according to the present invention includes a branch command determination circuit for determining whether the software command comprises a branch command or not every for execution processing of the software command, a branch command counter for adding in response to a branch command determination signal in this branch command determination circuit, a branch direction predicting circuit for outputting a branch direction prediction success signal when the branch direction of the branch command is identical with the branch direction indicated by a predicted value from the branch direction predicted value register on the basis of the determination result from the branch command determination circuit, a branch direction prediction success counter for counting the branch direction prediction success signal from this branch direction predicting circuit and obtaining the number of success of the branch direction prediction, a timer for clocking period of time in reference to a counting time of the branch direction prediction success and the branch direction prediction failure, a branch direction predicted value determination circuit for outputting a signal to switch the predicted branch direction of the branch direction predicted value when the number of the prediction success from the branch direction prediction

success counter which is counted during period of time indicated by this timer is compared with the number of prediction failure obtained by subtracting the number of the prediction success from the number of the branch commands from the branch command counter and this number of the prediction failure is more than the number of prediction success, and a branch direction predicted value register for storing the branch direction predicted value indicating the predicted branch direction and switching the branch predicted value to the direction of the failure when the signal is given to indicate that the number of the prediction failure from the branch direction predicted value determination circuit is more than the number of prediction success.

[0010]

[EMBODIMENT]

Next, an embodiment of the present invention will be explained in detail with reference to the drawings.

[0011]

With reference to FIG. 1, the first embodiment of the present invention includes a branch command determination circuit 1 for determining whether the software command, which is execution processing, comprises a branch command or not, a branch direction predicting circuit 2 for inputting the determination result from this branch command determination circuit 1 and the branch direction predicted value from a branch direction predicted value resistor 8 and outputting a branch direction prediction failure signal when the branch direction

of the branch command is not identical with the branch direction , which predicts the branch direction of the branch command and executes the branch command, a branch direction prediction failure counter 4 for inputting an unidentical signal indicating that the predicted branch direction obtained from this branch direction predicting circuit 2 is not identical with the executed branch direction, performing additional operation, counting the number of the branch direction prediction failure and being initialized by the signal from a branch direction predicted value determination circuit 7, a branch command counter 3, which is initialized by the signal from the branch direction predicted value determination circuit 7, for adding the number of the branch commands in response to the signal from the branch command determination circuit 1, a branch direction prediction measuring timer initial value register 5, which is capable of set the initial value of the timer arbitrarily by a micro-command or a shift-in operation, a branch direction prediction measuring timer 6 for subtracting the contents from this register 5, inputting the contents of the branch direction prediction measuring timer initial value register 5 and outputting the signal to the branch direction predicted value determination circuit 7 when the timer value is zero, the branch direction predicted value determination circuit 7 for comparing the value of the prediction success number, which is obtained by subtracting the value of the branch direction prediction failure counter 4 from the value of the branch command counter 3, with the value

of the prediction failure number of the branch direction prediction failure counter 4 in response to the input signal from this branch direction prediction measuring timer 6, outputting the branch direction predicted value controlling signal to the branch direction predicted value register 8 if the value of the prediction success number, which is obtained by subtracting the value of the branch direction prediction failure counter 4 from the value of the branch command counter 3, being smaller than the value of the prediction failure number of the branch direction prediction failure counter 4, and outputting the initialized controlling signal to the branch command counter 3 and the branch direction prediction failure counter 4 in response to the determination of the branch direction predicted value in any result, and the branch direction predicted value register 8 for inverting the stored value by the branch direction prediction controlling signal indicating the value of the prediction success number from the branch direction predicted value determination circuit 7 is smaller than the value of the prediction failure number to switch the branch predicted direction and storing the branch direction predicted value indicating the branch predicted direction.

[0012]

Next, the operation of the first embodiment of the present invention will be explained in detail with reference to the drawings.

[0013]

With reference to FIG. 1, the branch command determination circuit 1 inputs a bit pattern of the software command being execution processing and determining whether the software command comprises the branch command or not. If it comprises the branch command, the branch command determination circuit 1 outputs the signal to the branch direction predicting circuit 2 and the branch command counter 3. The branch direction predicting circuit 2 inputs the output signal of the branch command determination circuit 1 and the output signal of the branch direction predicted value register 8. If they are not identical with the branch direction of the branch command, which predicts and executes the branch direction of the branch command, the branch direction predicting circuit 2 outputs the signal to the branch direction prediction failure counter 4. The branch command counter 3 inputs the signal of the branch command determination circuit 1 and performs the additional operation. The contents of the branch command counter 3 is outputted to the branch direction predicted value determination circuit 7. Further, the contents of the branch command counter 3 is initialized by the input signal from the branch direction predicted value determination circuit 7. The branch direction prediction failure counter 4 inputs the signal of the branch direction predicting circuit 2 and performs the additional operation. The contents of the branch direction prediction failure counter 4 is outputted to the branch direction predicted value determination circuit 7. Further, the contents of the branch direction prediction failure counter

4 are initialized by the input signal from the branch direction predicted value determination circuit 7. The branch direction prediction measuring timer initial value register 5 is capable of arbitrarily writing by the micro command and the shift-in operation or the like. The contents of the branch direction prediction measuring timer initial value register 5 is outputted to the branch direction prediction measuring timer 6. The branch direction prediction measuring timer 6 has the same bit width as that of the branch direction prediction measuring timer initial value register 5 and performs a subtracting operation. Further, if the timer value becomes 0 by the subtracting operation, the branch direction prediction measuring timer 6 sets the contents of the branch direction prediction measuring timer initial value register 5 and outputs the signal to the branch direction predicted value determination circuit 7. The branch direction predicted value determination circuit 7 inputs the output signal of the branch command counter 3, the output signal of the branch direction prediction failure counter 4 and the output signal of the branch direction prediction measuring timer 6 to determine the branch direction predicted value. The determination of the branch direction predicted value is carried out by comparing the value obtained by subtracting the value of the branch direction prediction failure counter 4 from the value of the branch command counter 3 with the value of the branch direction prediction failure counter 4 with as a start of the input signal of the branch direction prediction measuring timer 6. If it

is found that the value obtained by subtracting the value of the branch direction prediction failure counter 4 from the value of the branch command counter 3 is smaller than the value of the branch direction prediction failure counter 4 from the result of the comparison, the branch direction predicted value determination circuit 7 outputs the branch direction predicted value controlling signal to the branch direction predicted value register 8. Further, if the direction predicted value is determined, the branch direction predicted value determination circuit 7 outputs the initialized controlling signal to the branch command counter 3 and the branch direction prediction failure counter 4. The branch direction predicted value register 8 inverts the stored value by the branch direction prediction controlling signal from the branch direction predicted value determination circuit 7 to store the branch direction predicted value. Further, the branch direction predicted value register 8 outputs the signal to control the
branch direction predicting circuit 2.

[0014]

Next, the operation of the second embodiment of the present invention will be explained in detail with reference to FIG. 2.

[0015]

With reference to FIG. 2, in the second embodiment of the present invention, the branch command determination circuit 1, the branch direction prediction failure counter 4,

the branch direction prediction measuring timer initial value register 5, the branch direction prediction measuring timer 6 and the branch direction predicted value register 8 have the same constructions as those of the first embodiment.

[0016]

A branch direction predicting circuit 2' compares the branch direction predicted value indicating the predicted branch direction, which is stored in the branch direction predicted value register 8 with the branch direction of the branch command, which is determined as the branch command in the branch command determination circuit 1. When the branch direction of the branch command is identical with the predicted branch direction, which is indicated by the branch direction predicted value, the circuit 2' outputs the prediction success signal to a branch direction prediction success counter 9. When the branch direction of the branch command is not identical with the predicted branch direction, which is indicated by the branch direction predicted value, the circuit 2' outputs the prediction failure signal to the branch direction prediction failure counter 4.

[0017]

The branch direction prediction success counter 9 is set to the initial value by the determination completion signal or the determination result signal from a branch direction predicted value determination circuit 10. The branch direction prediction success counter 9 counts the prediction success signal from the circuit 2' to output the number of the

prediction success.

[0018]

The branch direction predicted value determination circuit 10 is different from the branch direction predicted value determination circuit 7 of the first embodiment in the following points.

[0019]

In order to obtain the number of the prediction success, the branch direction predicted value determination circuit 7 of the first embodiment subtracts the number of the prediction failure, which is generated by the branch direction prediction failure counter 4 from the number of the branch commands, which is generated by the branch command counter 3.

[0020]

The above subtraction will be realized by performing an arithmetic operation with an arithmetic unit or the like.

[0021]

On the contrary, the branch direction predicted value determination circuit 10 of the second embodiment compares the number of the prediction success from the branch direction prediction success counter 9 with the number of the prediction failure from the branch direction prediction failure counter 4 to output the signal for switching the predicted direction of the branch direction predicted value, which is stored in the branch direction predicted value register 8 when the number of the prediction failure is more than the number of the prediction success.

[0022]

Next, with respect to the operation of the second embodiment of the present invention, the different points from the operation of the first embodiment will be explained with reference to FIG. 2.

[0023]

With reference to FIG. 2, the branch direction predicting circuit 2' outputs either the prediction success signal as the identical signal or the prediction failure signal as the disagreement signal.

[0024]

During the clocking period of the branch direction prediction measuring timer 6, the branch direction prediction success counter 9 and the branch direction prediction failure counter 4 operates in parallel and supply the number of the prediction success and the number of the prediction failure to the branch direction predicted value determination circuit 10. The branch direction predicted value determination circuit 10 saves the calculation of the number of the branch prediction success for itself by receiving the number of the branch prediction success number from the branch direction prediction success counter 9.

[0025]

Next, the operation of the third embodiment of the present invention will be explained in detail with reference to FIG. 3.

[0026]

With reference to FIG. 3, in the third embodiment of the present invention, the branch command determination circuit 1, the branch command counter 3, the branch direction prediction measuring timer initial value register 5, the branch direction prediction measuring timer 6 and the branch direction predicted value register 8 have the same constructions as the corresponding constructions of the first embodiment. Also, the branch direction prediction success counter 9 in the third embodiment of the present invention has the same construction as the corresponding construction of the second embodiment of the present invention. A branch direction predicting circuit 2'' in the third embodiment of the present invention outputs the prediction success signal when the branch direction of the branch command, which is determined in the branch command determination circuit 1, and the predicted branch direction, which is indicated by the predicted value stored in the branch direction predicted value register 8 are identical. This signal is given to the branch direction prediction success counter 9 to be used for countering the number of the prediction success.

[0027]

The number of the prediction success from the branch direction prediction success counter 9 and the number of the branch commands from the branch command counter 3 are given to a branch direction predicted value determination circuit 7'. On this account, the branch direction predicted value determination circuit 7' subtracts the number of the prediction

success from the number of the branch commands to calculate the number of the prediction failure. When this number of the prediction failure is more than the number of the prediction success, the branch direction predicted value determination circuit 7' outputs the signal indicating this result. This signal is used to change the branch direction of the predicted value stored in the branch direction predicted value register 8 as same as the embodiments of the first and the second embodiments.

[0028]

Next, the features of the operation of the third embodiment of the present invention will be explained.

[0029]

According to the branch direction predicting circuits 2, 2' and 2'' through the first to the third embodiments, the branch direction of the branch command, which is determined in the branch command determination circuit 1, is checked. This branch direction is capable of being represented by the binary directions or the binary numerals such as four directions or the like. Accordingly, this branch direction is capable of being determined due to decoding the OP code of the command.

[0030]

Comparing the branch direction of the branch command with the branch direction, which is indicated by the predicted value from the branch direction predicted value register 8, if they are identical, the branch direction predicting circuit 2'' of the third embodiments outputs the prediction success signal

to the branch direction prediction success counter 9.

[0031]

The branch direction predicted value determination circuit 7' subtracts the output from the branch direction prediction success counter 9 and the number of the prediction success from the number of the branch commands of the time period, which is clocked by the timer 6, to obtain the number of the prediction failure. Next, the branch direction predicted value determination circuit 7' compares the obtained number of the prediction failure with the number of the prediction success from the branch direction prediction success counter 9. If the number of the prediction failure is more than the prediction success, the branch direction predicted value determination circuit 7' supplies the signal indication this result to the branch direction predicted value register 8. The branch direction predicted value register 8 switches the predicted branch direction, which is indicated by the predetermined value, with this signal.

[0032]

[EFFECT OF THE INVENTION]

In the present invention, changing the branch direction predicting direction of the branch command dynamically on the information processing apparatus for predicting the branch direction of the branch command and performing the branch direction predicting success processing at higher speed than the branch direction predicting failure processing on the basis of the number of the branch direction prediction success of

the branch command, which is practically executed, allows the present invention to have an effect that a difference in processing time of the program depending on the branch command using method of the program becomes small and it becomes unnecessary to create the program, which considers the branch direction of the branch command in order to process the program at a high speed.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[FIG. 1]

FIG. 1 shows a first embodiment according to the present invention.

[FIG. 2]

FIG. 2 shows a second embodiment according to the present invention.

[FIG. 3]

FIG. 3 shows a third embodiment according to the present invention.

[DESCRIPTION OF REFERENCE NUMERALS]

1: branch command determination circuit

2: branch direction predicting circuit

3: branch command counter

4: branch direction prediction failure counter

5: branch direction prediction measuring timer initial value register

6: branch direction prediction measuring timer

7: branch direction predicted value determination circuit

8: branch direction predicted value register

9: branch direction prediction success counter

10: branch direction predicted value determination circuit

FIG. 1

SOFTWARE COMMAND BIT PATTERN

1: BRANCH COMMAND DETERMINATION CIRCUIT

2: BRANCH DIRECTION PREDICTING CIRCUIT

3: BRANCH COMMAND COUNTER

4: BRANCH DIRECTION PREDICTION FAILURE COUNTER

5: BRANCH DIRECTION PREDICTION MEASURING TIMER INITIAL VALUE REGISTER

6: BRANCH DIRECTION PREDICTION MEASURING TIMER

7: BRANCH DIRECTION PREDICTED VALUE DETERMINATION CIRCUIT

8: BRANCH DIRECTION PREDICTED VALUE REGISTER

FIG. 2

SOFTWARE COMMAND BIT PATTERN

1: BRANCH COMMAND DETERMINATION CIRCUIT

2': BRANCH DIRECTION PREDICTING CIRCUIT

9: BRANCH DIRECTION PREDICTION SUCCESS COUNTER

4: BRANCH DIRECTION PREDICTION FAILURE COUNTER

5: BRANCH DIRECTION PREDICTION MEASURING TIMER INITIAL VALUE REGISTER

6: BRANCH DIRECTION PREDICTION MEASURING TIMER

10: BRANCH DIRECTION PREDICTED VALUE DETERMINATION CIRCUIT

8: BRANCH DIRECTION PREDICTED VALUE REGISTER

FIG. 3

SOFTWARE COMMAND BIT PATTERN

1: BRANCH COMMAND DETERMINATION CIRCUIT

2'': BRANCH DIRECTION PREDICTING CIRCUIT

3: BRANCH COMMAND COUNTER

9: BRANCH DIRECTION PREDICTION SUCCESS COUNTER

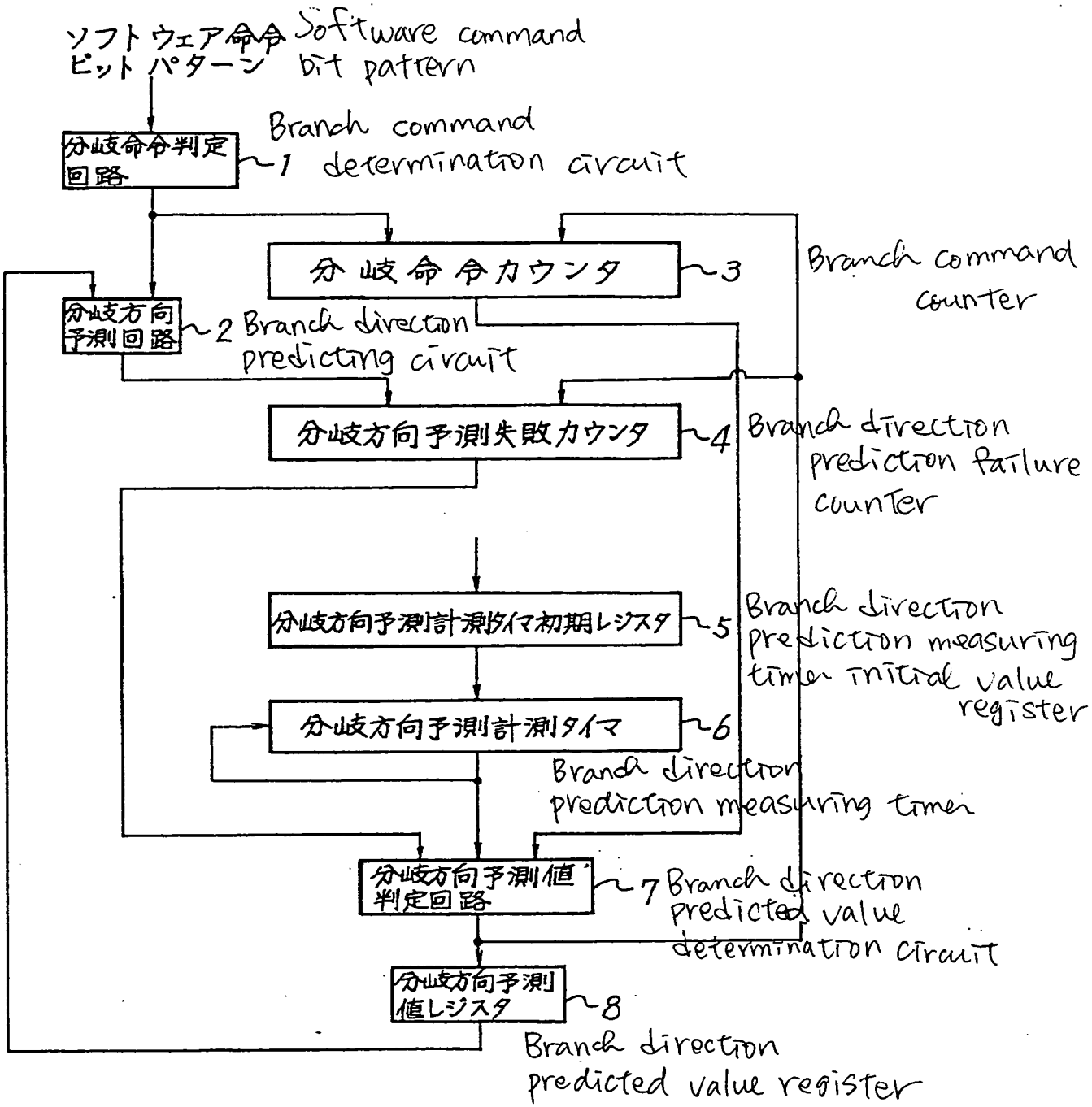
5: BRANCH DIRECTION PREDICTION MEASURING TIMER INITIAL VALUE REGISTER

6: BRANCH DIRECTION PREDICTION MEASURING TIMER

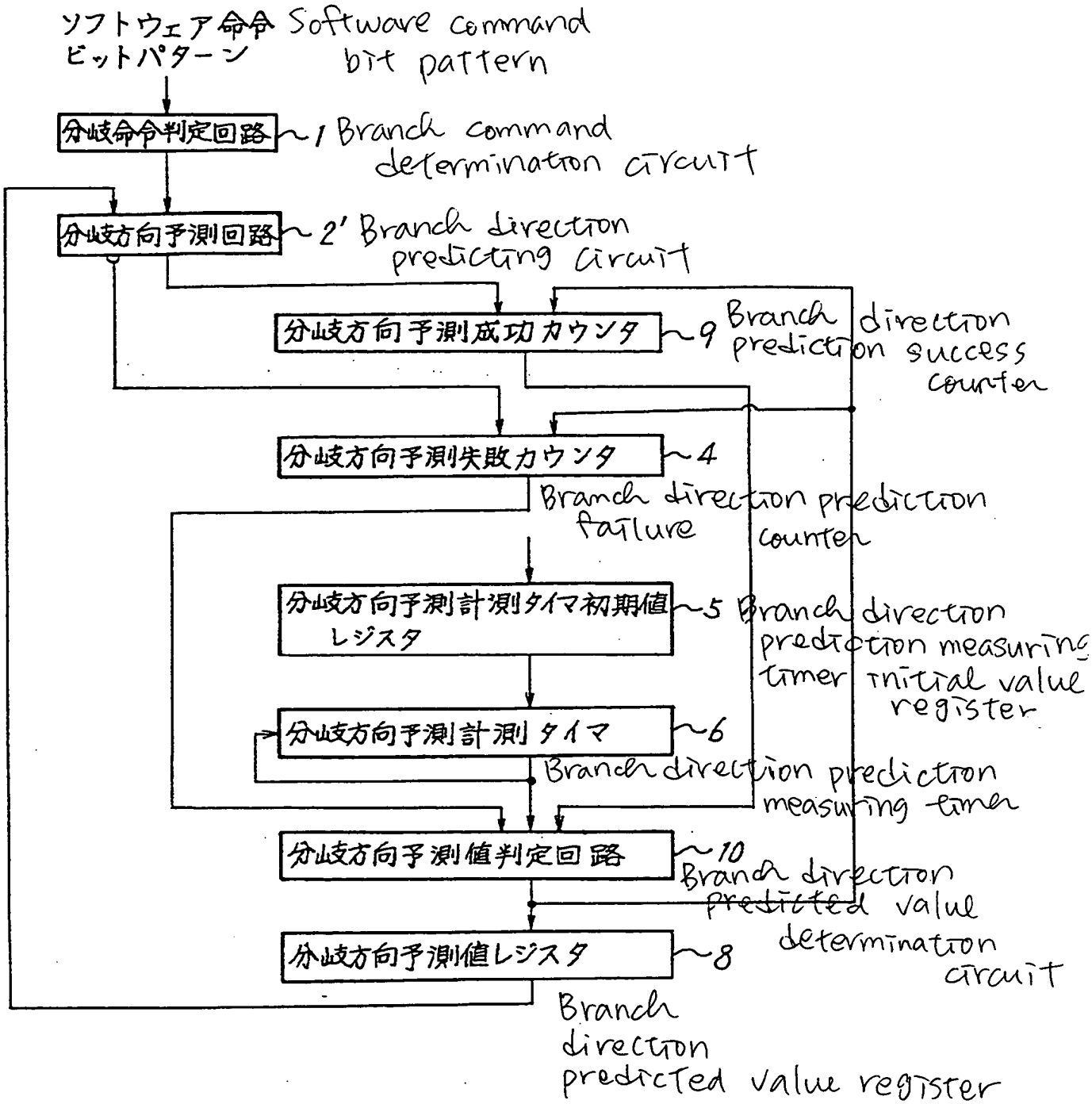
7': BRANCH DIRECTION PREDICTED VALUE DETERMINATION CIRCUIT

8: BRANCH DIRECTION PREDICTED VALUE REGISTER

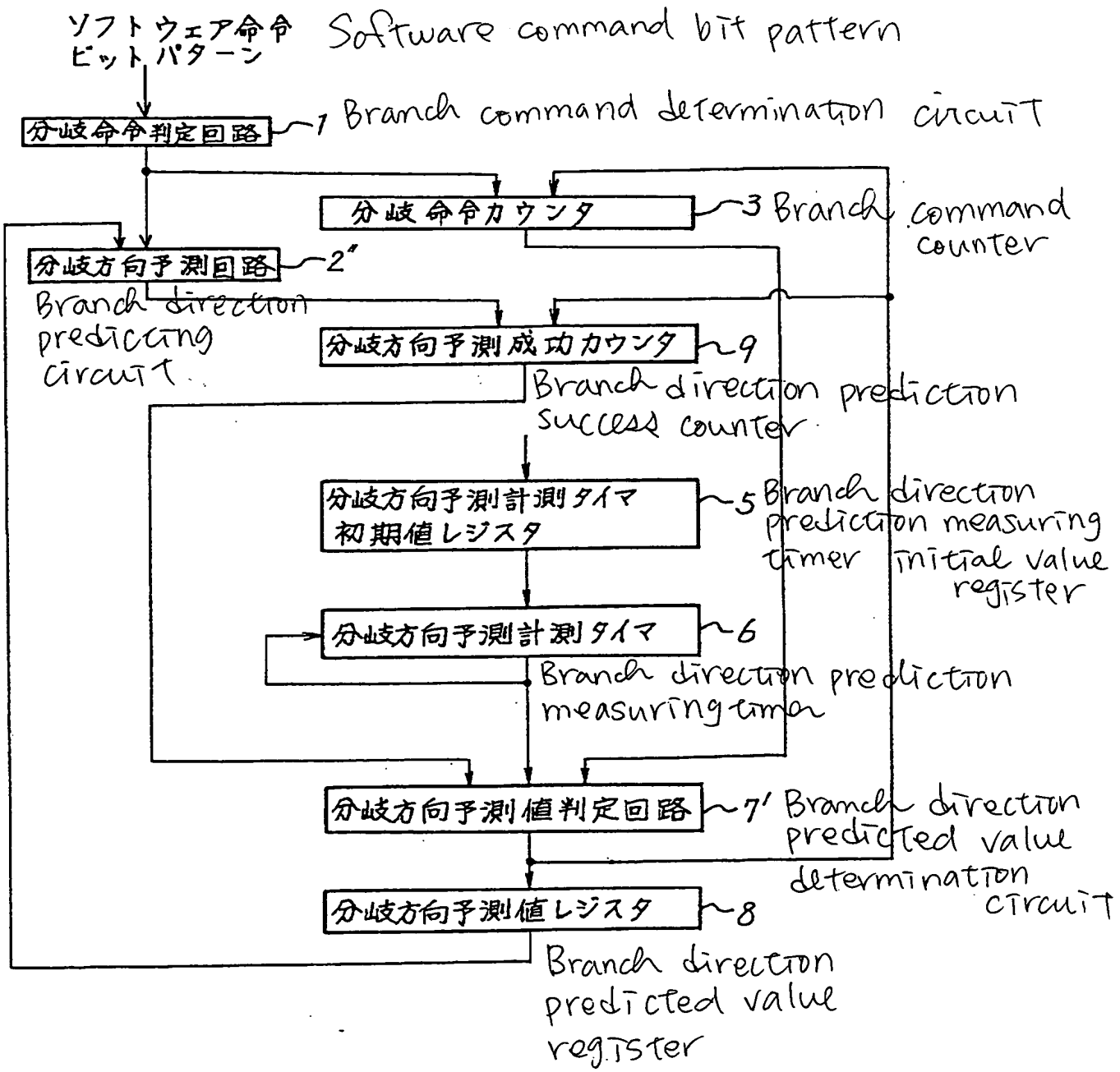
【図１】


ソフトウェア命令ビットパターン
Software command bit pattern
分岐命令判定回路
1
Branch command determination circuit
分岐命令カウンタ
3
Branch command counter
分岐方向予測回路
2
Branch direction predicting circuit
分岐方向予測失敗カウンタ
4
Branch direction prediction failure counter
分岐方向予測計測タイマ初期レジスタ
5
Branch direction prediction measuring timer initial value register
分岐方向予測計測タイマ
6
Brand direction prediction measuring timer
分岐方向予測値判定回路
7
Branch direction predicted value determination circuit
分岐方向予測値レジスタ
8
Branch direction predicted value register

【図2】


ソフトウェア命令ビットパターン
Software command bit pattern
分岐命令判定回路
1 Branch command determination circuit
分岐方向予測回路
2' Branch direction predicting circuit
分岐方向予測成功カウンタ
9 Branch direction prediction success counter
分岐方向予測失敗カウンタ
4 Branch direction prediction failure counter
分岐方向予測計測タイマ初期値レジスタ
5 Branch direction prediction measuring timer initial value register
分岐方向予測計測タイマ
6 Branch direction prediction measuring timer
分岐方向予測値判定回路
10 Branch direction predicted value determination circuit
分岐方向予測値レジスタ
8 Branch direction predicted value register

【図３】


ソフトウェア命令ビットパターン
Software command bit pattern
分岐命令判定回路
1 Branch command determination circuit
分岐命令カウンタ
3 Branch command counter
分岐方向予測回路
2″
Branch direction predicting circuit
分岐方向予測成功カウンタ
9
Branch direction prediction success counter
分岐方向予測計測タイマ初期値レジスタ
5 Branch direction prediction measuring timer initial value register
分岐方向予測計測タイマ
6
Branch direction prediction measuring timer
分岐方向予測値判定回路
7′ Branch direction predicted value determination circuit
分岐方向予測値レジスタ
8
Branch direction predicted value register

(19)日本国特許庁(JP)　(12)公開特許公報（A）　(11)特許出願公開番号

特開平6－324866

(43)公開日　平成6年(1994)11月25日

(51)Int. Cl.[5]	識別記号	庁内整理番号	F I	技術表示箇所
G06F 9/38		330 B		

審査請求　有　請求項の数4　OL　（全8頁）

(21)出願番号　特願平5-102070

(22)出願日　平成5年(1993)4月28日

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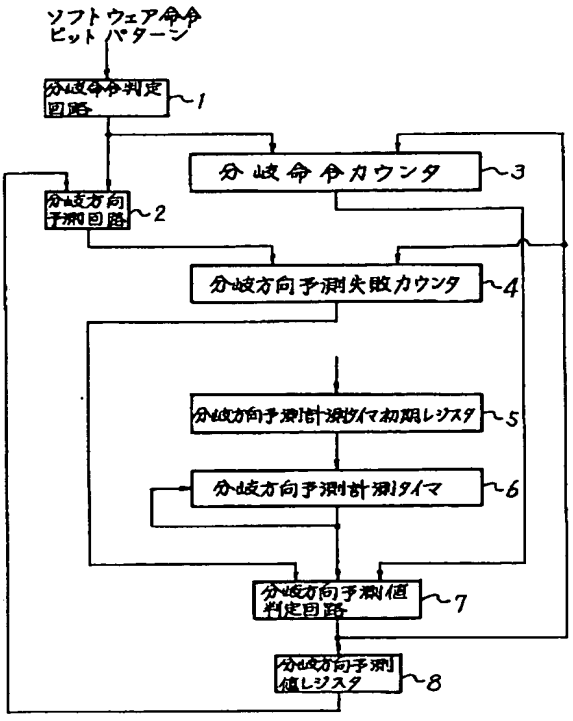
(54)【発明の名称】分岐方向予測動的変更装置

(57)【要約】

【目的】実行履歴のない分岐命令の分岐方向予測を行う場合に、プログラムの分岐命令使用方法による、分岐命令の分岐方向予測の成功率の低下による処理速度の低下を防ぐ。

【構成】分岐方向予測値判定回路７は、分岐方向予測計測タイマ６からの入力信号を契機に分岐命令カウンタ３の値から分岐方向予測失敗カウンタ４の値を引いた値と分岐方向予測失敗カウンタ４の値を比較し、比較結果が分岐命令カウンタ３の値から分岐方向予測失敗カウンタ４の値を引いた値が分岐方向予測失敗カウンタ４の値より小さければ分岐方向予測値レジスタ８へ分岐方向予測値制御信号を出力する。



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【特許請求の範囲】

【請求項１】　分岐命令の分岐方向の予測値を格納する分岐方向予測値格納手段と、

この分岐方向予測値格納手段からの予測値で示される分岐方向と処理される分岐命令の分岐方向とを比較する分岐方向予測手段と、

この分岐方向予測手段からの信号に基づいて予測失敗回数と予測成功回数との少なくとも一方を計数する回数計数手段と、

この回数計数手段からの計数値に基づき一定計測時間内に予測失敗回数が予測成功回数より大きいか否かを判定し分岐方向予測値格納手段に格納された分岐方向予測値の予測分岐方向を切換えるため予測失敗回数が予測成功回数より大きいことを示す信号を出力する分岐方向予測値判定手段とを含むことを特徴とする分岐方向予測動的変更装置。

【請求項２】　実行処理ごとに命令が分岐命令か否かを判定する分岐命令判定手段と、

この分岐命令判定手段での判定結果に応答して分岐命令の数を計数する分岐命令計数手段とを備え、

前記回数計数手段は予測失敗回数を計数し、

前記分岐方向予測値判定手段は前記分岐命令計数手段で計数された分岐命令数から前記回数計数手段で計数された予測失敗回数を差し引いて予測成功回数を求め、求められた予測成功回数が前記予測失敗回数より小さいか否かを判定することを特徴とする請求項１記載の分岐方向予測動的変更装置。

【請求項３】　前記回数計数手段は予測失敗回数と予測成功回数との両方を計数し、

前記分岐方向予測値判定手段は一定計測時間内に前記回数計数手段から与えられる予測失敗回数が前記回数計数手段から与えられる予測成功回数より大きいか否かを判定することを特徴とする請求項１記載の分岐方向予測動的変更装置。

【請求項４】　実行処理ごとに命令が分岐命令か否かを判定する分岐命令判定手段と、

この分岐命令判定手段での判定結果に応答して分岐命令の数を計数する分岐命令計数手段とを備え、

前記回数計数手段は予測成功回数を計数し、

前記分岐方向予測値判定手段は前記分岐命令計数手段で計数された分岐命令数から前記回数計数手段で計数された予測成功回数を差し引いて予測失敗回数を求め、求められた予測失敗回数が前記予測成功回数より大きいか否かを判定することを特徴とする請求項１記載の分岐方向予測動的変更装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は分岐命令の分岐方向予測を行い分岐方向予測成功処理を分岐方向予測失敗処理より高速に実行する情報処理装置上で分岐命令の分岐方向予測方向を動的に変更する分岐方向予測動的変更装置に関する。

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【０００２】

【従来の技術】従来この種の分岐方向予測は、特開平３－７３０２２号公報に示されている。図６に示されているように、一般的なプログラムでは同一箇所の分岐命令において再度分岐する確率が高いことを利用し、分岐予測回路が用いられている。さらに、プログラムの特色である『後方分岐は繰返し発生する確率が大』、『前方分岐の繰返しの確率はプログラムによることが大きい』ということを利用し、分岐命令のアドレスと分岐先のアドレスとを比較している。

【０００３】また、初めて実行され以前の分岐方向が不明の分岐命令については、情報処理装置のハードウェアが固定的に分岐方向の予測を行なっていた。

【０００４】

【発明が解決しようとする課題】一般に分岐命令の分岐方向予測は、ソフトウェア命令実行を高速に処理するために行われ、分岐方向予測が失敗した場合、分岐方向予測が成功した場合に比べ処理は遅くなる。

【０００５】上述した従来の分岐命令の分岐方向予測において、ハードウェアが固定的に分岐方向の予測を行う場合は、同じ論理のプログラムであってもプログラムの分岐命令使用方法によりプログラムの処理時間に差ができる。したがって、高速処理するようにプログラムを作成する場合ハードウェアが固定的に分岐方向を予測する分岐命令の分岐方向を考慮して分岐命令を使用しなければならないという欠点がある。

【０００６】

【課題を解決するための手段】上述の課題を解決するため、本発明の第１の分岐方向予測動的変更装置は、分岐命令の分岐方向の予測値を格納する分岐方向予測値レジスタと、この分岐方向予測値レジスタからの予測値で示される分岐方向と処理される分岐命令の分岐方向とを比較する分岐方向予測回路と、この分岐方向予測回路からの信号に基づいて予測失敗回数と予測成功回数との少なくとも一方を計数するカウンタと、このカウンタからの計数値に基づき一定計測時間内に予測失敗回数が予測成功回数より大きいか否かを判定し分岐方向予測値レジスタに格納された分岐方向予測値の予測分岐方向を切換えるため予測失敗回数が予測成功回数より大きいことを示す信号を出力する分岐方向予測値判定回路とを含む。

【０００７】上述の課題を解決するための、本発明の第２の分岐方向予測動的変更装置は、ソフトウェア命令の実行処理ごとにソフトウェア命令が分岐命令かどうか判定する分岐命令判定回路と、この分岐命令判定回路での分岐命令判定信号に応答して加算する分岐命令カウンタと、分岐命令判定回路からの判定結果にもとづいて分岐命令の分岐方向が分岐方向予測値レジスタからの予測値の示す分岐方向と一致していないとき分岐方向予測失敗

信号を出力する分岐方向予測回路と、この分岐方向予測回路からの分岐方向予測失敗信号を計数し分岐方向予測の失敗回数を求める分岐方向予測失敗カウンタと、分岐方向予測成功と分岐方向予測失敗の計測時間に関し一定時間を計時するタイマと、このタイマで示される時間内にカウントされる分岐方向予測失敗カウンタからの予測失敗回数および分岐命令カウンタからの分岐命令数から予測失敗回数を差し引くことにより得られる予測成功回数を比較しこの予測失敗回数が予測成功回数より大きければ分岐方向予測値の予測分岐方向を切換えるための信号を出力する分岐方向予測値判定回路と、予測分岐方向を示す分岐方向予測値を格納し、前記分岐方向予測値判定回路からの予測失敗回数が予測成功回数より大きい旨を示す信号を与えられたときその失敗方向に分岐予測値を切換える分岐方向予測値レジスタとを含む。

【０００８】本発明の第３の分岐方向予測動的変更装置は、ソフトウェア命令の実行処理ごとにソフトウェア命令が分岐命令か否か判定する分岐命令判定回路と、この分岐命令判定回路からの判定結果にもとづいて分岐命令の分岐方向が分岐方向予測値レジスタからの予測値と一致していないとき分岐方向予測失敗信号を出力し一致しているとき分岐方向予測成功信号を出力する分岐方向予測回路と、この分岐方向予測回路からの分岐方向予測失敗信号を計数し分岐方向予測の失敗回数を求める分岐方向予測失敗カウンタと、前記分岐方向予測回路からの分岐方向予測成功信号を計数し分岐方向予測の成功回数を求める分岐方向予測成功カウンタと、分岐方向予測成功と分岐方向予測失敗の計測時間に関し一定時間を計時するタイマと、このタイマで示される時間内にカウントされる前記分岐方向予測失敗カウンタからの予測失敗回数と前記分岐方向予測成功カウンタからの予測成功回数とを比較しこの予測失敗回数が予測成功回数より大きければ分岐方向予測値の予測分岐方向を切換える信号を出力する分岐方向予測値判定回路と、予測分岐方向を示す分岐方向予測値を格納し前記分岐予測値判定回路からの予測失敗回数が予測成功回数より大きいことを示す信号により分岐方向予測値の予測分岐方向を切換える分岐方向予測値レジスタ８とを含む。

【０００９】本発明の第４の分岐方向予測動的変更装置は、ソフトウェア命令の実行処理ごとにソフトウェア命令が分岐命令かどうか判定する分岐命令判定回路と、この分岐命令判定回路での分岐命令判定信号に応答して加算する分岐命令カウンタと、分岐命令判定回路からの判定結果にもとづいて分岐命令の分岐方向が分岐方向予測レジスタからの予測値の示す分岐方向と一致するとき分岐方向予測成功信号を出力する分岐方向予測回路と、この分岐方向予測回路からの分岐方向予測成功信号を計数し分岐方向予測の成功回数を求める分岐方向予測成功カウンタと、分岐方向予測成功と分岐方向予測失敗の計測時間に関し一定時間を計時するタイマと、このタイマで

示される時間内にカウントされる分岐方向予測成功カウンタからの予測成功回数および分岐命令カウンタからの分岐命令数から予測成功回数を差し引くことにより得られる予測失敗回数を比較しこの予測失敗回数が予測成功回数より大きければ分岐方向予測値の予測分岐方向を切換えるための信号を出力する分岐方向予測値判定回路と、予測分岐方向を示す分岐方向予測値を格納し分岐方向予測値判定回路からの予測失敗回数が予測成功回数より大きい旨の信号を与えられたときその失敗方向に分岐予測値を切換える分岐方向予測値レジスタとを含む。

【００１０】

【実施例】次に本発明の一実施例について図面を参照して詳細に説明する。

【００１１】図１を参照すると、本発明の第１の実施例は、処理実行中のソフトウェアが分岐命令か否かを判定する分岐命令判定回路１、この分岐命令判定回路１からの判定結果と分岐方向予測値レジスタ８からの分岐方向予測値とを入力し分岐命令の分岐方向を予測し実行した分岐命令の分岐方向と一致しなければ分岐方向予測失敗信号を出力する分岐方向予測回路２、この分岐方向予測回路２から与えられる予測分岐方向と実行分岐方向との不一致信号を入力し加算動作を行い、分岐方向予測失敗回数を計数し分岐方向予測値判定回路７からの信号により初期化される分岐方向予測失敗カウンタ４、分岐方向予測値判定回路７からの信号により初期化され分岐命令判定回路１からの信号に応答して分岐命令の数を加算する分岐命令カウンタ３、マイクロ命令またはシフトイン動作でタイマの初期値を任意に設定できる分岐方向予測計測タイマ初期値レジスタ５、このレジスタ５からの内容を減算し、タイマ値がゼロになると分岐方向予測計測タイマ初期値レジスタ５の内容を入力するとともに分岐方向予測値判定回路７に信号を出力する分岐方向予測計測タイマ６、この分岐方向予測計測タイマ６からの入力信号に応答して分岐命令カウンタ３の値から分岐方向予測失敗カウンタ４の値を引いた予測成功回数値と分岐方向予測失敗カウンタ４の予測失敗回数値とを比較し、命令カウンタ３の値から分岐方向予測失敗カウンタ４の値を引いた予測成功回数値が分岐方向予測失敗カウンタ４の予測失敗回数値より小さければ分岐方向予測値レジスタ８へ分岐方向予測値制御信号を出力するとともに、結果のいかんを問わず分岐方向予測値の判定に応答して分岐命令カウンタ３および分岐方向予測失敗カウンタ４へ初期化制御信号を出力する分岐方向予測値判定回路７およびこの分岐方向予測値判定回路７からの予測成功回数値の予測失敗回数値より小なることを示す分岐方向予測制御信号により格納値を反転して分岐予測方向を切替え、分岐予測方向を示す分岐方向予測値を格納する分岐方向予測値レジスタ８を含む。

【００１２】次に本発明の第１の実施例の動作について図面を参照して詳細に説明する。

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【００１３】図１を参照すると、分岐命令判定回路１は、処理実行中のソフトウェア命令のビットパターンを入力とし分岐命令かどうか判定を行い、分岐命令であれば分岐方向予測回路２と分岐命令カウンタ３へ信号を出力する。分岐方向予測回路２は、分岐命令判定回路１の出力信号と分岐方向予測値レジスタ８の出力信号を入力とし分岐命令の分岐方向を予測し実行した分岐命令の分岐方向と一致しなければ分岐方向予測失敗カウンタ４へ信号を出力する。分岐命令カウンタ３は、分岐命令判定回路１の信号を入力信号として加算動作を行う。分岐命令カウンタ３の内容は、分岐方向予測値判定回路７へ出力する。さらに分岐方向予測値判定回路７からの入力信号により初期化される。分岐方向予測失敗カウンタ４は、分岐方向予測回路２の信号を入力信号として一加算動作を行う。分岐方向予測失敗カウンタ４の内容は、分岐方向予測値判定回路７へ出力する。さらに分岐方向予測値判定回路７からの入力信号により初期化される。分岐方向予測計測タイマ初期値レジスタ５は、マイクロ命令及びシフトイン動作等で任意に書込みができる。分岐方向予測計測タイマ初期値レジスタ５の内容は、分岐方向予測計測タイマ６へ出力する。分岐方向予測計測タイマ６は、分岐方向予測計測タイマ初期値レジスタ５と同一のビット幅を持ち減算動作を行う。さらに減算動作によりタイマ値がゼロになると分岐方向予測計測タイマ初期値レジスタ５の内容を設定し分岐方向予測値判定回路７へ信号を出力する。分岐方向予測値判定回路７は、分岐命令カウンタ３の出力信号と分岐方向予測失敗カウンタ４の出力信号と分岐方向予測計測タイマ６の出力信号を入力とし分岐方向予測値を判定する。分岐方向予測値の判定は、分岐方向予測計測タイマ６からの入力信号を契機に分岐命令カウンタ３の値から分岐方向予測失敗カウンタ４の値を引いた値と分岐方向予測失敗カウンタ４の値を比較することで行われる。比較した結果が命令カウンタ３の値から分岐方向予測失敗カウンタ４の値を引いた値が分岐方向予測失敗カウンタ４の値より小さければ分岐方向予測値レジスタ８へ分岐方向予測値制御信号を出力する。さらに分岐方向予測値の判定が行われた場合は、分岐命令カウンタ３及び分岐方向予測失敗カウンタ４へ初期化制御信号を出力する。分岐方向予測値レジスタ８は、分岐方向予測値判定回路７からの分岐方向予測値制御信号により格納値を反転し分岐方向予測値を格納する。さらに分岐方向予測値レジスタ８は、分岐方向予測回路２の制御のため信号を出力する。

【００１４】次に本発明の第２の実施例について図２を参照して詳細に説明する。

【００１５】図２を参照すると、本発明の第２の実施例において分岐命令判定回路１，分岐方向予測失敗カウンタ４，分岐方向予測計測タイマ初期値レジスタ５，分岐方向予測計測タイマ６、および分岐方向予測値レジスタ８は第１の実施例と同じ構成である。

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【００１６】分岐方向予測回路２′は、分岐方向予測値レジスタ８に格納された予測分岐方向を示す分岐方向予測値と分岐命令判定回路１で分岐命令と判定された分岐命令の分岐方向とを比較する。分岐命令の分岐方向と分岐方向予測値の示す予測分岐方向とが一致したとき、回路２′は予測成功信号を分岐方向予測成功カウンタ９に出力する。分岐命令の分岐方向と分岐方向予測値の示す予測分岐方向とが一致しないとき、回路２′は予測失敗信号を分岐方向予測失敗カウンタ４に出力する。

【００１７】分岐方向予測成功カウンタ９は、分岐方向予測値判定回路１０からの判定終了または判定結果信号により初期値に設定され、回路２′からの予測成功信号を計数し予測成功回数を出力する。

【００１８】分岐方向予測値判定回路１０は、以下の点で第１の実施例における分岐方向予測判定回路７とは異なる。

【００１９】第１の実施例における分岐方向予測判定回路７では予測成功回数を求めるために、分岐命令カウンタ３で生成された分岐命令数から分岐方向予測失敗カウンタ４で生成された予測失敗回数を差し引いている。

【００２０】この減算は演算器等で演算すれば実現される。

【００２１】これに対し第２の実施例における分岐方向予測判定回路１０では、分岐方向予測成功カウンタ９からの予測成功回数と分岐方向予測失敗カウンタ４からの予測失敗回数とを比較し予測失敗回数が予測成功回数より大きいとき分岐方向予測値レジスタ８に格納された分岐方向予測値の予測方向を切換えるための信号を出力する。

【００２２】次に本発明の第２の実施例の動作について第１の実施例の動作と異なる点を図２を参照して説明する。

【００２３】図２を参照すると、分岐方向予測回路２′は一致信号である予測成功信号か不一致信号である予測不成功信号かのどちらか一方を出力する。

【００２４】分岐方向予測計測タイマ６の計時期間中、分岐方向予測成功カウンタ９と分岐方向予測失敗カウンタ４とは並行動作し、予測成功回数と予測失敗回数とを判定回路１０に供給する。分岐方向予測値判定回路１０は分岐方向予測成功回数をカウンタ９から受けとることにより自ら分岐方向予測成功回数の計算を省略している。

【００２５】次に本発明の第３の実施例について図３を参照して詳細に説明する。

【００２６】図３を参照すると、本発明の第３の実施例における分岐命令判定回路１，分岐命令カウンタ３，分岐命令方向予測計測タイマ初期値レジスタ５，分岐方向予測計測タイマ６，分岐方向予測値レジスタ８は、本発明の第１の実施例における対応する構成と同一である。また、本発明の第３の実施例における分岐方向予測成功

カウンタ９は、本発明の第２の実施例における対応する構成と同一である。本発明の第３の実施例における分岐方向予測回路２″は分岐命令判定回路１で判定された分岐命令の分岐方向と分岐方向予測値レジスタ８に格納された予測値で示される予測分岐方向との一致がとれたときに予測成功信号を出力する。この信号は分岐方向予測成功カウンタ９に与えられ、予測成功回数の計測に使われる。

【００２７】分岐方向予測判定回路７′には、分岐方向予測成功カウンタ９からの予測成功回数と分岐命令カウンタ３からの分岐命令数とが与えられる。このため、回数７′は分岐命令数から予測成功回数を差し引いて予測失敗回数を計算し、この予測失敗回数が予測成功回数より大きいとき、その旨を示す信号を出力する。この信号は第１および第２の実施例と同様分岐方向予測値レジスタ８に格納された予測値の分岐方向を変えるために使われる。

【００２８】次に本発明の第３の実施例の動作について特徴となる点を説明する。

【００２９】第１～第３の実施例を通して分岐方向予測回路２，２′および２″では、分岐命令判別回路１で判別された分岐命令の分岐方向をみる。この分岐方向は２方向又は４方向等２進数字で表現でき、命令のＯＰコードを解読することにより判別可能である。

【００３０】この第３の実施例の分岐方向予測回路２″ではこの分岐命令の分岐方向と分岐方向予測値レジスタ８からの予測値で示される分岐方向とを比較し一致していれば予測成功信号をカウンタ９に対し出力する。

【００３１】分岐方向予測値判定回路７′は、タイマ６により計時される時間帯の分岐命令数から予測成功カウンタ９の出力、予測成功回数を差し引いて予測失敗回数

を求める。次に判定回路７′は、求められた予測失敗回数と予測成功カウンタ９からの予測成功回数とを比較し、予測失敗回数が予測成功回数より大きいときはその旨を示す信号を分岐方向予測値レジスタ８に与える。分岐方向予測値レジスタ８は、この信号により予測値の示す予測分岐方向を切換える。

【００３２】

【発明の効果】本発明は、分岐命令の分岐方向予測を行い分岐方向予測成功処理を分岐方向予測失敗処理より高速に実行する情報処理装置上で実際に実行した分岐命令の分岐方向予測成功数をもとに分岐方向予測方向を動的に変更することにより、プログラムの分岐命令使用方法によるプログラム処理時間の差が小さくなり、プログラム高速処理のための分岐命令の分岐方向を考慮したプログラム作成は不要となるという効果がある。

【図面の簡単な説明】

【図１】本発明の第１の実施例を示す図である。

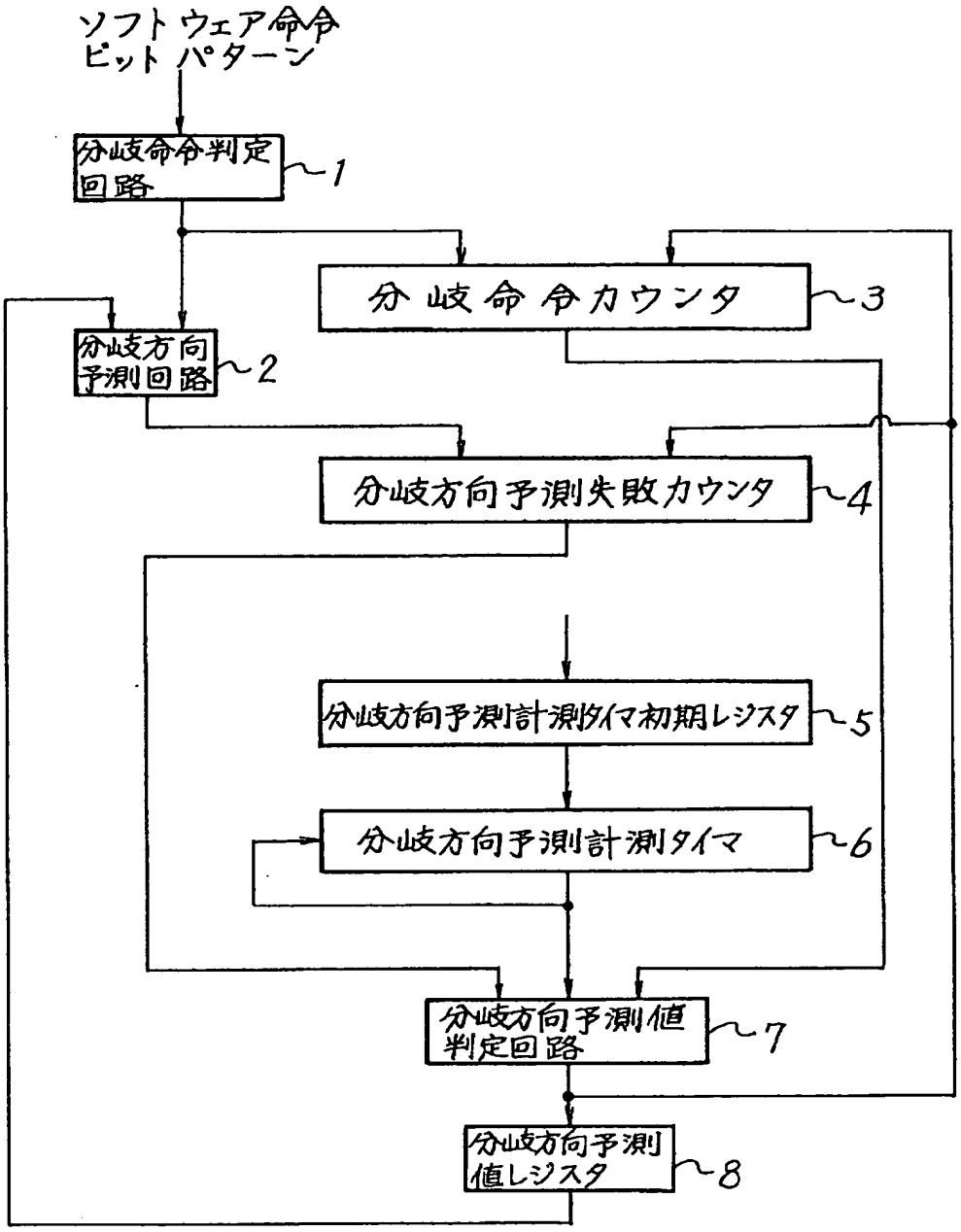
【図２】本発明の第２の実施例を示す図である。

【図３】本発明の第３の実施例を示す図である。

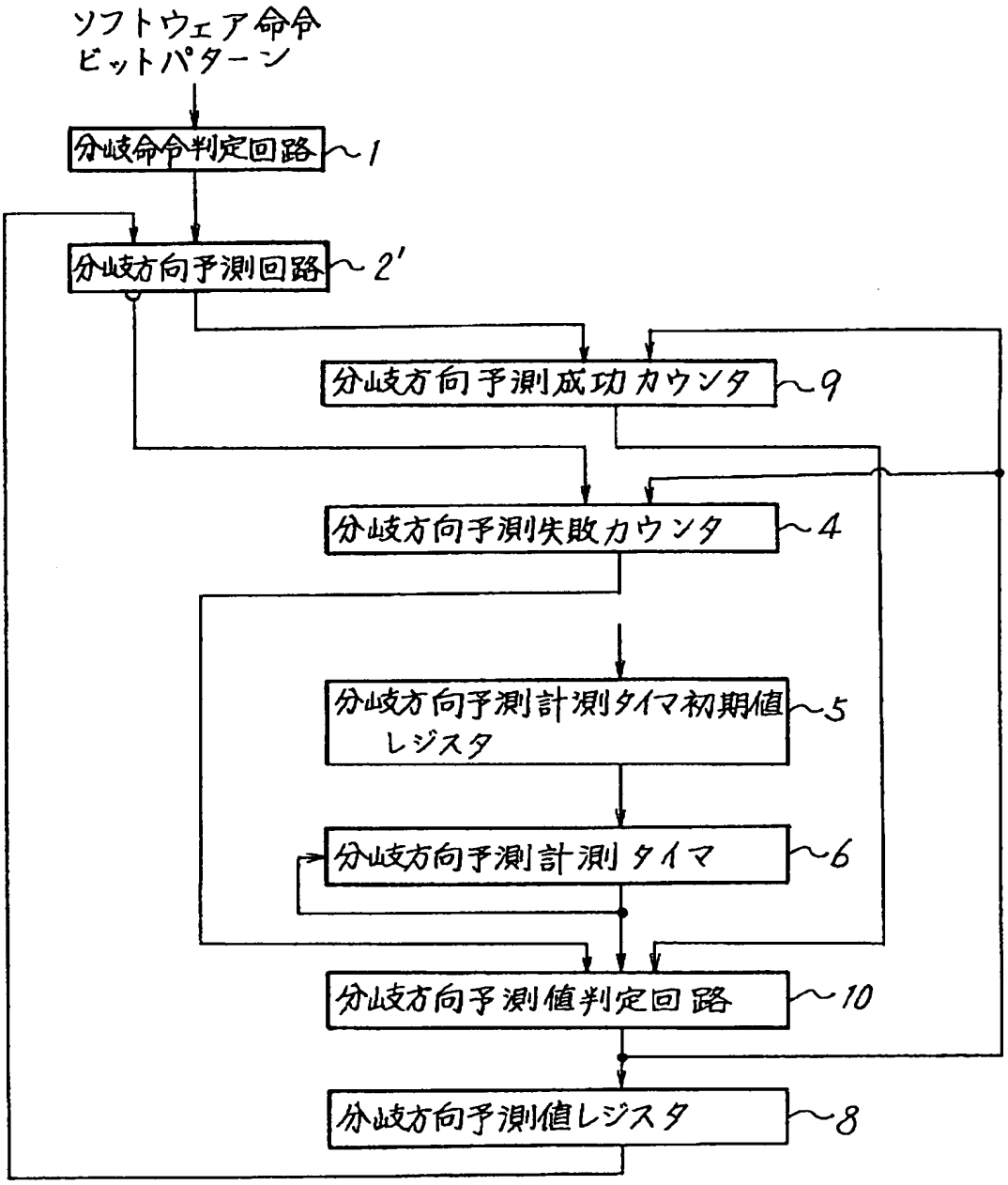
【符号の説明】

１　分岐命令判定回路
２　分岐方向予測回路
３　分岐命令カウンタ
４　分岐方向予測失敗カウンタ
５　分岐方向予測計測タイマ初期値レジスタ
６　分岐方向予測計測タイマ
７　分岐方向予測値判定回路
８　分岐方向予測値レジスタ
９　分岐方向予測成功カウンタ
１０　分岐方向予測判定回路

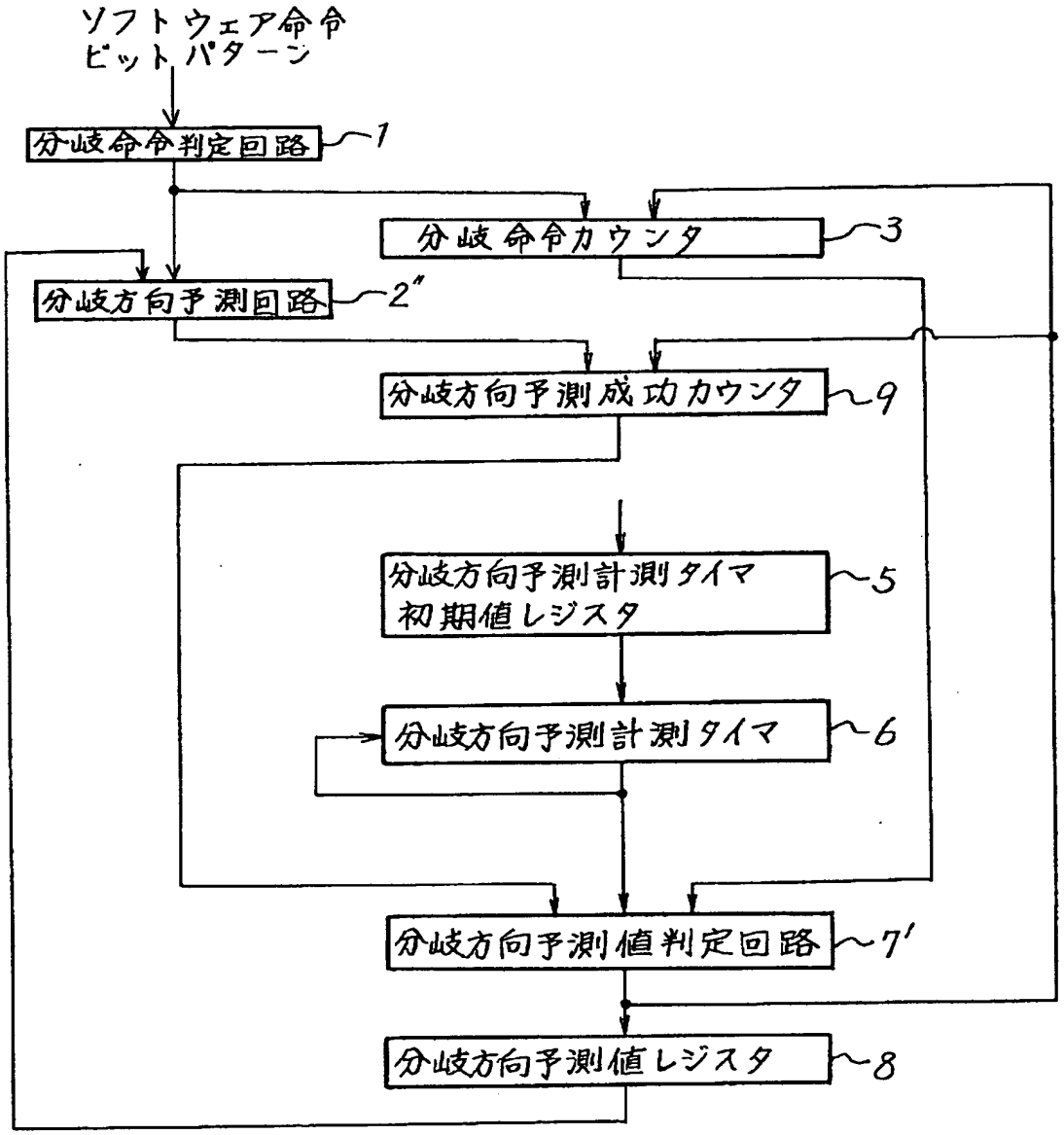
【図１】


ソフトウェア命令
ビットパターン
分岐命令判定回路
1
分岐命令カウンタ
3
分岐方向予測回路
2
分岐方向予測失敗カウンタ
4
分岐方向予測計測タイマ初期レジスタ
5
分岐方向予測計測タイマ
6
分岐方向予測値判定回路
7
分岐方向予測値レジスタ
8

【図２】


ソフトウェア命令
ビットパターン
分岐命令判定回路
1
分岐方向予測回路
2'
分岐方向予測成功カウンタ
9
分岐方向予測失敗カウンタ
4
分岐方向予測計測タイマ初期値
レジスタ
5
分岐方向予測計測タイマ
6
分岐方向予測値判定回路
10
分岐方向予測値レジスタ
8

【図３】


ソフトウェア命令
ビットパターン
分岐命令判定回路
1
分岐命令カウンタ
3
分岐方向予測回路
2″
分岐方向予測成功カウンタ
9
分岐方向予測計測タイマ
初期値レジスタ
5
分岐方向予測計測タイマ
6
分岐方向予測値判定回路
7′
分岐方向予測値レジスタ
8